

JPL D-27604

Start Up Read Only Memory (SUROM)

Non-Volatile Memory Functional Requirements

Version 1.0

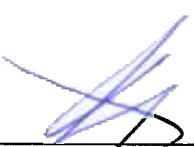
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SUROM

Non-Volatile Memory

Functional Requirements

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1 Purpose and Scope

1.1 Purpose

This document defines functional requirements for replacement and upgrade of an existing Start Up Read Only Memory (SUROM).

1.2 Scope

This document defines the requirements needed for a non-volatile memory that will replace and upgrade the 128 kBytes of SUROM on an existing processor board.

It is the goal of this development to generate a product that is a form, fit, and functional replacement of an existing product but with additional radiation hardness – allowing rapid substitution without a loss in overall system performance.

1.3 Description

The SUROM Upgrade will be a component that meets all the requirements and thus allows for replacement of existing components.

The SUROM Upgrade will allow for 1 Mbit, organized as 128 K x 8 bits, of nonvolatile memory for program storage.

1.4 Applicability

This document is applicable to all procurements of identical product.

2 Applicable Documents

The following documents are applicable:

2.1 Project Documents

JPL 982-00025, "Draft JIMO Parts Program Requirements"

JPL 982-00037, "Draft JIMO Reliability Assurance Requirements"

2.2 JPL Documents

2.3 NASA/Military Documents

2.4 Industry Standards & Documents

JEP122-B - "Failure Mechanisms and Models for Semiconductor Devices"

JESD91-A - "Method for Development of Acceleration Models for Electronic Components and Failure Mechanisms"

2.5 Commercial Documents

Renesas Semiconductor, HN58C1001 1Mbit EEPROM specification,
document ADE-203-028G(Z), Rev 7.0, Oct. 1997

2.6 Order of Precedence

In case of conflict, the following order of precedence applies:

1. Contract Requirements
2. Technical Direction Memorandum
3. JPL Standards & Requirements
4. Functional Requirements
5. Contractor developed Specification
6. Industry Standards & Requirements
7. Commercial Specifications

3 REFERENCE DOCUMENT

The following is included for reference purposes.

3.1 Project Documents

JPL 982-00029 Draft JIMO Environmental Requirements Document,
dated 1/12/2004

4 Index of Abbreviations and Terms

4.1 Non-Volatility

Non-Volatility is that which is retained in memory by a means such that the removal of power does not alter or delete stored data.

4.2 kByte

A kiloByte is 8192 individual bits.

4.3 Mbit

A Megabit is 1,048,576 individual bits.

4.4 Bit Error Rate

Bit Error Rate (BER) is defined as the total number of detected errors experienced per unit time.

4.5 Radiation Hardened

Radiation Hardened devices are ones that experience no degradation whatsoever following exposure to a specified Total Dose and Energetic Particle environment – usually to some extreme value.

4.6 Capacity

It is important to note that throughout this document, data storage figures represent the minimums required for data storage only and do not take into account:

- additional memory elements required for an implementation of device-internal error detection and correction (EDAC)

Additional memory elements required due to the above reasons are *over and above* any capacity requirement mentioned within this document.

4.7 “Write Cycle Limited”

A device is said to be Write Cycle limited when the number of times a memory cell may be reliably written to is limited to some number by the design and physics of the device itself.

4.8 “Write Cycle Reads”

It is recognized that, in devices where cell-fatigue is an issue, the fatigue of the cell may actually be experienced during a Read cycle instead of – or in addition to – a Write cycle. For the purposes of this document, there shall be an assumed equivalency between Write cycle and Read cycle cell-fatigue.

It is further recognized that some devices used may experience a self-generated Write cycle (*viz.* cell data regeneration) as a result of a Read. Should the aforementioned Read cycle cause fatigue, then the number of Write Cycles required in subsequent paragraphs of this document dealing with cell life, shall be increased to allow for the minimum specified number of write cycles to be achieved.

4.9 Erasure Cycle Writes

Some devices utilize or require a block erasure prior to the instantiation of new data in a cell or block of cells. Should this erasure be stressful to the cell, then the erasure shall be not considered *in addition to* the following write cycle.

Should a Write Cycle following erasure not impose additional cell stress, then that Write cycle shall be counted against the maximum number of Writes allowed.

4.10 [Bracketed Number]

Throughout this document, certain numbers appear inside brackets “[n]”. The bracketing of a number indicates that the number, while considered reasonable and proper, is subject to review and change.

4.11 Lower case n appended to signal names

Throughout this document, certain signal names (functional signals and pin definitions) appear with a lower case “n” appended to the end of the signal name. This indicated that the signal being defined is active low true signal type. An example would be a Chip Enable signal denoted CE. CE itself would be an active high true signal (logic level ‘1’ true, whereas CEn is an active low true signal (logic level ‘0’ true).

5 Configuration Requirements

The SUROM shall be fabricated in three distinct hardware phases. The definitions of the three Phases are as follows.

5.1 Phase 1

A unit produced for a Phase 1 development has the same device rules, processing and speed as a device proposed for phase 2, but not necessarily the same capacity or packaging.

A Phase 1 unit is one which complies functionally with the requirements of section 6 and 7.

A Phase 1 unit will not be subjected to environmental operating requirements outside of room ambient conditions.

Phase 1 units shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in section 8.3.

Phase 1 units shall be marked with a C - NNN designator, where NNN is a number from 001 to the maximum number of Phase 1 units manufactured.

5.2 Phase 2

A Phase 2 unit is one which complies with all functional and test requirements in sections 6, 7, 8, and 10.

Phase 2 units shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in section 8.3.

Phase 2 units delivered shall be marked with a B - NNN quality Designator, where NNN is a number from 001 to the maximum number of Phase 2 units manufactured.

5.3 Phase 3

A Phase 3 unit is one that complies with all requirements in sections 6 thru 10.

Additionally, Phase 3 units shall be tested to requirements of JPL 982-00025.

Phase 3 units shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in section 8.3.

Phase 3 units delivered shall be marked with an A -NNN quality Designator, where NNN is a number from 001 to the maximum number of Phase 3 units manufactured.

6 Functional Requirements

The SUROM shall contain electronics and circuitry to meet the functional requirements defined in this section.

The SUROM shall be verified by test and analysis as required to perform within specification as stated in this section when subjected to the Environment specified in §8.

Compliance to the requirements of §7 shall be by analysis.

Compliance to the requirements of §10 shall be by test.

6.1 Device Emulation

The SUROM upgrade shall emulate to the maximum extent possible the operation of a Renesas HN58C1001 1Mbit EEPROM while showing compliance with additional requirements and definitions described elsewhere in this document. Deviation from this requirement shall be clearly identified.

6.2 Functional Signal implementation

In basic terms, the SUROM shall be consistent with the functional signals shown in Figure 1.

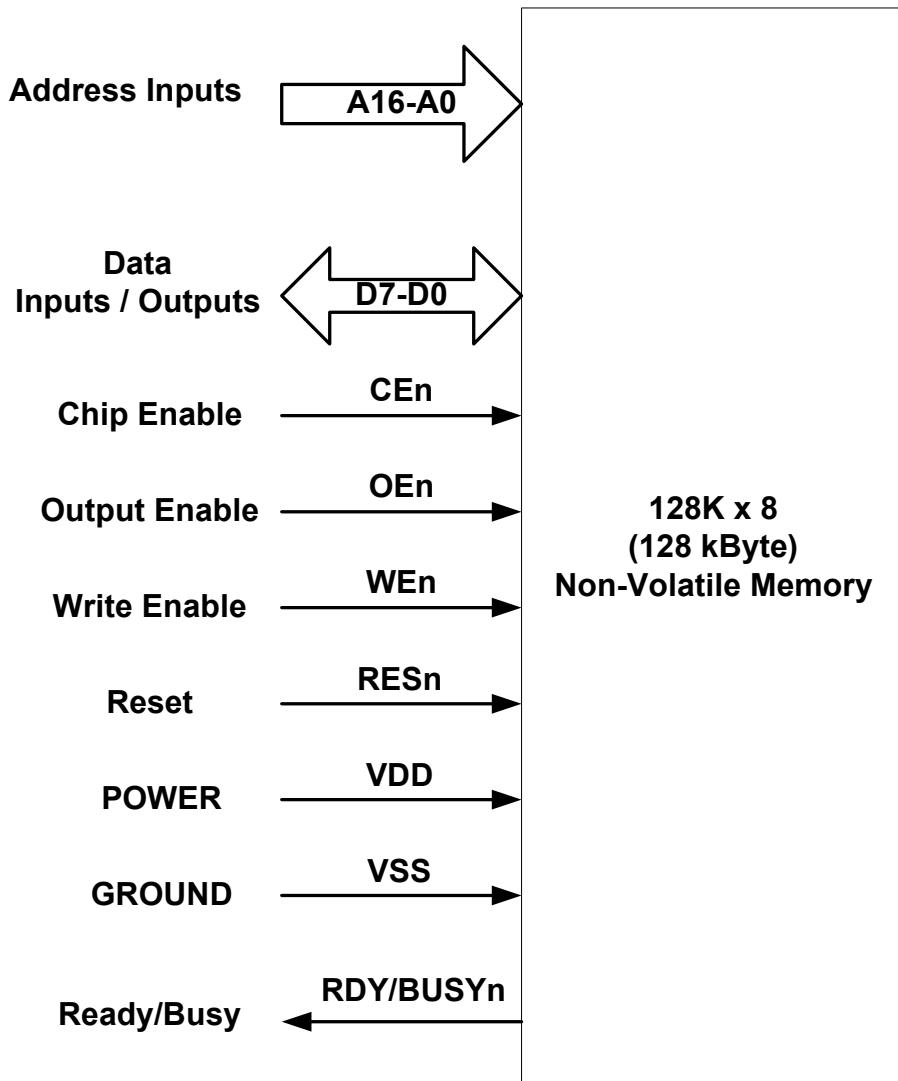


Figure 1 – Functional Signal Implementation

6.2.1 Function to Pin Mapping

The SUROM functional pin definitions shall map to the functional signal definition as defined in Table 1.

Table 1 – Signal Function to Pin definition map

FUNCTIONAL SIGNAL NAME	FUNCTIONAL PIN NAME
Address Inputs	A16 – A0
Data Input / Outputs	D7 – D0
Chip Enable Input	CEn
Output Enable Input	OEn
Write Enable Input	WE _n
Reset Input	RES _n
Ready/Busy Output	RDY/BUSY _n
Power Input	VDD
Ground	VSS

6.2.2 Pin Electrical Characteristics

The SUROM signal pins shall have the electrical characteristics defined in Table 2.

Table 2 – Pin Electrical Characteristics

(T_A = 25 °C, F = 1 MHz)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
Input Leakage Current	V _{DD} = 3.6V, V _{IN} = 3.6V	I _{LI}	-	2 ¹	µA
Output Leakage Current	V _{DD} = 3.6V, V _{OUT} = 3.6V	I _{LO}	-	2	µA
Input Voltage		V _{IL} V _{IH} V _H	- 2.0 ² V _{DD} -0.5	0.8 - -	V
Output Voltage	I _{OL} = 2.1mA I _{OL} = -0.4mA I _{OL} = -0.1mA	V _{OL} V _{OH} V _{OH}	- V _{DD} ×0.8 V _{DD} -0.3	0.4 - -	V
Input Capacitance	V _{IN} = 0V	C _{IN}	-	6	pF
Output Capacitance	V _{OUT} = 0V	C _{OUT}	-	12	pF

1. I_{LI} on RES = 100 µA max.

2. V_{IH} min = 2.2 V for V_{DD} = 3.6 V.

6.2.3 Operational Mode Selection

The SUROM shall permit reading and writing of a single byte when selected by the signal combinations defined in Table 3.

Table 3 – Mode Selection^{1,2}

MODE	CEn	OEn	WE _n	RES	RDY/BUSY _n	DATA
Read	V _{IL}	V _{IL}	V _{IH}	V _H	High-Z	D _{OUT}
Standby	V _{IH}	X	X	X	High-Z	High-Z
Write	V _{IL}	V _{IH}	V _{IL}	V _H	High-Z --> V _{OL}	D _{IN}
Deselect	V _{IL}	V _{IH}	V _{IH}	V _H	High-Z	High-Z
Write Inhibit	X	X	V _{IH}	X	-	-
	X	V _{IL}	X	X	-	-
Data Polling	V _{IL}	V _{IL}	V _{IH}	V _H	V _{OL}	D _{OUT} (D7)
Program	X	X	X	V _{IL}	High-Z	High-Z

1. X = Don't care.

2. Refer to the recommended DC operating values.

6.2.4 Memory Capacity

Each memory package shall contain 1 Mbit of memory for data storage organized in byte wide fashion (128 K x 8).

6.2.5 Operational Lifetime

Compliance to this requirement shall be by test and analysis. Methods and methodology as prescribed in JESD91 and JEP122 shall be used. Operational Lifetime shall include, as a minimum, temperature and radiation effects.

6.2.5.1 Write/Erase Cycles

Devices developed to this document shall support a minimum of 10000 Write/Erase Cycles in the specified environment.

6.2.5.2 Device Lifetime, powered

Devices developed to this document shall operate within specification for a period of 20 years.

6.2.5.3 Data Retention

Devices developed to this document shall be able to successfully read --- during and after exposure to the environments specified in §8 --- data stored within for a period of no less than 15 years after being written.

6.2.5.3.1 Data Refresh

The use of externally operated, controlled, or initiated data refresh to achieve the data retention requirement is prohibited.

Devices using internal data refresh:

1. Shall be fully accessible by the host at all times
2. Shall demonstrate compliance with the Bit Error Rates stated in §8.3.2 during and after the data refresh
3. Shall not decrease required unit lifetime and shall not include the number of refresh cycles required to achieve retention requirements for the Write/Erase cycles specified in this section.

6.2.6 AC Electrical Characteristics

Each SUROM pin shall meet the AC characteristics defined in Table 4 and Table 5 while being tested with the following conditions

- Input rise and fall time: ≤ 20 ns
- Output load: 1 TTL Gate + 100pF
- Input & output waveforms and reference levels as per Table 2

6.2.6.1 Read cycle timing

Each memory package shall adhere to read cycle timing defined in Table 4. (Ref. Renesas data sheet)

Table 4 – AC Electrical Characteristics for Read Operation

($V_{DD} = 3.3 \text{ V} \pm 10\%$, $T_A = -55 \text{ to } 125^\circ\text{C}$ (Unless otherwise specified))

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT
Address Access Time	$\text{CEn} = \text{OEn} = V_{IL}, \text{WE}_n = V_{IH}$	t_{ACC}	-	200	ns
Chip Enable Access Time	$\text{OEn} = V_{IL}, \text{WE}_n = V_{IH}$	t_{CE}	-	200	ns
Output Enable Access Time	$\text{CEn} = V_{IL}, \text{WE}_n = V_{IH}$	t_{OE}	0	110	ns
Output Hold to Address Change	$\text{CEn} = \text{OEn} = V_{IL}, \text{WE}_n = V_{IH}$	t_{OH}	0	-	ns
Output Disable to High-Z ¹	$\text{CEn} = V_{IL}, \text{WE}_n = V_{IH}$	t_{DF}	0	50	ns
Output Disable to High-Z ¹	$\text{CEn} = \text{OEn} = V_{IL}, \text{WE}_n = V_{IH}$	t_{DFR}	0	300	ns
RESn to Output Delay	$\text{CEn} = \text{OEn} = V_{IL}, \text{WE}_n = V_{IH}$	t_{RR}	0	525	ns

1. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.

6.2.6.2 Write and Erase cycle Timing

Each memory package shall adhere to write and erase cycle timing defined in Table 5. (Ref. Renesas data sheet)

Table 5 – AC Electrical Characteristics for Erase and Write Operations
 $(V_{DD} = 3.3 \text{ V} \pm 10\%, T_A = -55 \text{ to } 125 \text{ }^\circ\text{C}$ (Unless otherwise specified))

PARAMETER	SYMBOL	MIN	MAX	UNIT
Address Setup Time	t_{AS}	0	-	ns
Chip Enable to Write Setup Time (WEn controlled)	t_{CS}	0	-	ns
Write Pulse Width (CEn controlled)	t_{CW}	200	-	ns
Write Pulse Width (WEn controlled)	t_{WP}	200	-	ns
Address Hold Time	t_{AH}	125	-	ns
Data Setup Time	t_{DS}	100	-	ns
Data Hold Time	t_{DH}	10	-	ns
Chip Enable Hold Time (WEn controlled)	t_{CH}	0	-	ns
Write Enable to Write Setup Time (CEn controlled)	t_{WS}	0	-	ns
Write Enable Hold Time (CEn controlled)	t_{WH}	0	-	ns
Output Enable to Write Setup Time	t_{OES}	0	-	ns
Output Enable Hold Time	t_{OEH}	0	-	ns
Write Cycle Time ¹	t_{WC}	-	15	ms
Byte Load Cycle	t_{BLC}	1	30	μs
Data Latch Time	t_{DL}	700	-	ns
Byte Load Window	t_{BL}	100	-	μs
Time to Device Busy	t_{DB}	100	-	ns
Write Start Time	t_{DW}	150	-	ns
RESn to Write Setup Time	t_{RP}	100	-	μs
V_{DD} to RESn Setup Time	t_{RES}	1	-	μs

1. t_{WC} must be longer than this value unless polling techniques or RDY/BUSYn are used. The device must automatically complete the write operation within this time value.

6.2.7 Additional Function Definitions

Not notwithstanding functions described elsewhere, the SUROM shall have the operations defined below.

6.2.7.1 Automatic page write

The SUROM shall allow for automatic page writes to memory similar to the Renesas HN58C1001. The SUROM shall allow for writes of 1 to 128 Bytes in a single write cycle. Following an initial Byte write cycle, additional 1 to 127 write cycles shall be allowed before data is written into the SUROM.

6.2.7.2 WEn, CEn Pin Operation

During a write cycle, addresses shall be latched by the falling edge of WEn or CEn, and data shall be latched by the rising edge of WEn or CEn.

6.2.7.3 DATA_n Polling

DATA_n polling shall allow the status of the SUROM to be determined.

6.2.7.4 RDY/BUSY_n signal

RDY/BUSY_n signal shall allows for the status of the SUROM to be determined.

6.2.7.5 RESn Signal

When the RESn signal is low, the SUROM cannot be read or written. Data shall be protected when RESn is low, even if voltage applied to V_{DD} (relative to V_{SS}) is between specified values of V_{DD(max)} and V_{SS} for any duration. RESn shall be kept high during read and write operations.

6.2.7.6 Device Data Protection

6.2.7.6.1 Noise protection

Protection of device from entering program mode due to noisy control lines during data read or standby shall be implemented by ignoring control pulse widths of less than 20 ns during programming mode.

6.2.7.6.2 Power Cycling data protection

The SUROM shall not require specific sequences of power and application of control signals during power-up or power-down periods, to prevent to the corruption of data contained within. See also §6.2.7.6.4.

6.2.7.6.3 Software Data Protection

To prevent unintentional programming, the SUROM device shall have a software data protection (SDP) mode.

6.2.7.6.4 Under voltage write lockout

If the voltage difference between V_{DD} and V_{SS} is less than [2.5] volts the SUROM shall not allow any write functions to occur. The SUROM shall have an internal reference that allows for detection of this under-voltage condition.

6.2.8 Power

6.2.8.1 Operating Voltage, V_{DD}

The SUROM shall require only one voltage to be externally supplied: V_{DD} . The SUROM shall be fully operational over the Power Input voltage range of $V_{DD} = 3.3 \pm 10\%$ volts, DC. Except as specified elsewhere, successful reading from, or writing of data to, the SUROM when the power input voltage is out of the specified range is not guaranteed.

6.2.8.2 Maximum Current

The maximum current consumable by an SUROM package is defined as follows:

6.2.8.2.1 Operating

During device operation, maximum package current required by the SUROM (phase 2 and phase 3 parts) shall not exceed [50] mA. The current required by the phase 1 parts shall not exceed [50] mA.

6.2.8.2.2 Standby

During device standby ($CEn = \text{High}$), the maximum package current required by the SUROM (phase 2 and phase 3 parts) shall not exceed [15] mA at 150 nS cycle time. The current required by the phase 1 parts shall not exceed [15] mA at 150 ns cycle time.

6.2.8.2.3 Absolute Maximum Voltage

The absolute maximum voltage to be applied to the part is 5.5 volts $V_{DD} - V_{SS}$ and 0.7 volts above V_{DD} on any signal pin.

7 Design Prohibitions

This section details design prohibitions.

7.1 Power Source

The SUROM shall not rely on power stored internally for the purposes of data retention. Power shall be applied only by the external source specified in §6.2.8.

7.2 Moving Parts

The SUROM shall have no moving parts.

7.3 Trapped Logic States

Logical states for which there is no exit except power off are prohibited.

8 Environmental Design Requirements

The SUROM shall be designed and tested to meet the Environmental Requirements specified below.

8.1 Requirements Applicable to All Tests at Temperature

All operational requirements as specified in §6 shall apply at any operating temperature as stated below.

8.2 Design, Analysis, and Test Temperature Limits

8.2.1 Design and Analysis

The SUROM shall be designed and analyzed to meet the following temperature range: -55C to +125C.

8.2.2 Test

Phase 2 and 3 components shall be tested for operation within specification as defined in §6 over a temperature range of -55C to +125C.

Phase 3 components shall also be tested to satisfy the requirements of JPL 982-00025.

8.2.2.1 Margin Testing

Phase 2 Units subjected to margin testing requirements as specified in the procurement contract shall be tested for operation at a combination of low and high voltage extremes and low and high temperature extremes. Testing to parametric failure (i.e. specification non-compliance) outside of the voltage and temperature limits specified in §6.2.8.1 and §8.2.2 shall be performed.

8.3 Radiation

Devices developed to this document shall show operation within specification during and after exposure to the Ionizing Radiation environment specified when tested according to JPL 982-00025.

8.3.1 Radiation Total Ionizing Dose

A demonstration of compliance within specification following exposure to a minimum of 300 krad_(Si) TID at the die level, without shielding, is required.

Operation within specification following exposure to 1Mrad_(Si) TID at the die level, minimum, without shielding, is a goal.

8.3.2 Single Event Effects

Components shall be designed, analyzed, and tested for Single Event Effects per the requirements of JPL 982-00025.

8.3.2.1 Bit Error Rate

Data upset shall not exceed 1e-10 bit errors per day for all causes (SEE, SEFI, address error), measured after EDAC.

8.3.2.2 Active Latch Up Mitigation

The use of active circuitry to mitigate a Latchup condition shall be verified by test and analysis, subject to review and acceptance by JPL.

9 Parts Quality Requirements

Notwithstanding other requirements stated herein, devices manufactured to this document for Phase 3 shall comply or shall contain components that comply with JPL 982-00025.

10 Mechanical Design Requirements

10.1 Recommended Package Dimensions

The recommended package for the SUROM is shown below. See Figure 2 and Table 6.

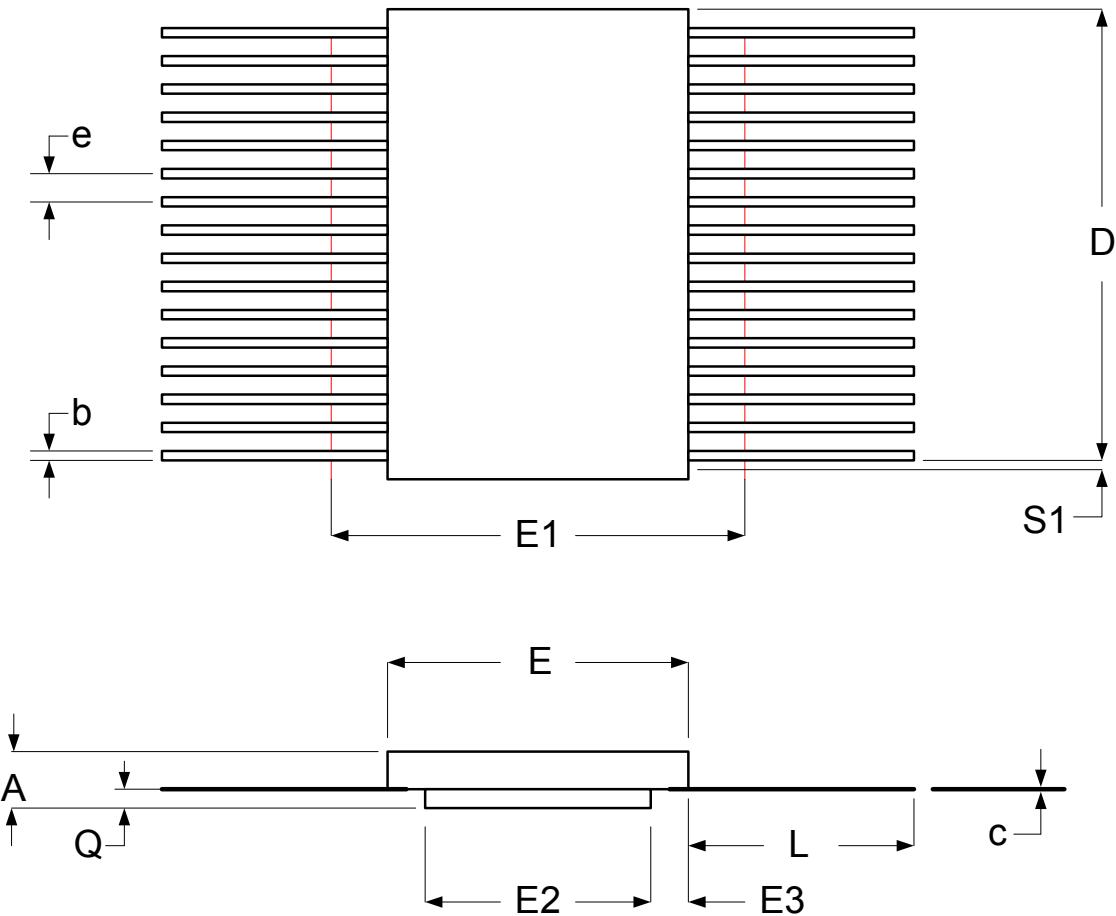


Figure 2 – Recommended Mechanical Package Diagram

Table 6 – Recommended Mechanical Package Dimensions

SYMBOL	DIMENSION (mm)		
	MINIMUM	NOMINAL	MAXIMUM
A	3.07	3.40	3.73
b	0.38	0.43	0.56
c	0.10	0.13	0.23
D	--	20.83	21.08
E	11.99	12.19	12.40
E1	--	--	12.65
E2	7.72	7.87	--
E3	0.76	2.16	--
e	1.27BSC		
L	9.02	9.27	9.53
Q	0.51	0.89	1.14
S1	0.13	0.69	--
# of pins	32		

10.2 Mass

Mass of a SUROM component shall not exceed [7.4] grams.

11 SUROM Support Equipment

[Reserved]

12 Notes

12.1 Units of Measurement

All drawings and calculations submitted shall use the International System of Units (SI) {MKS metric system}.

12.2 Contractors and Subcontractors

Requirements specified in this document are applicable to designs and products produced by the Contractor and any subcontractor utilized therein.